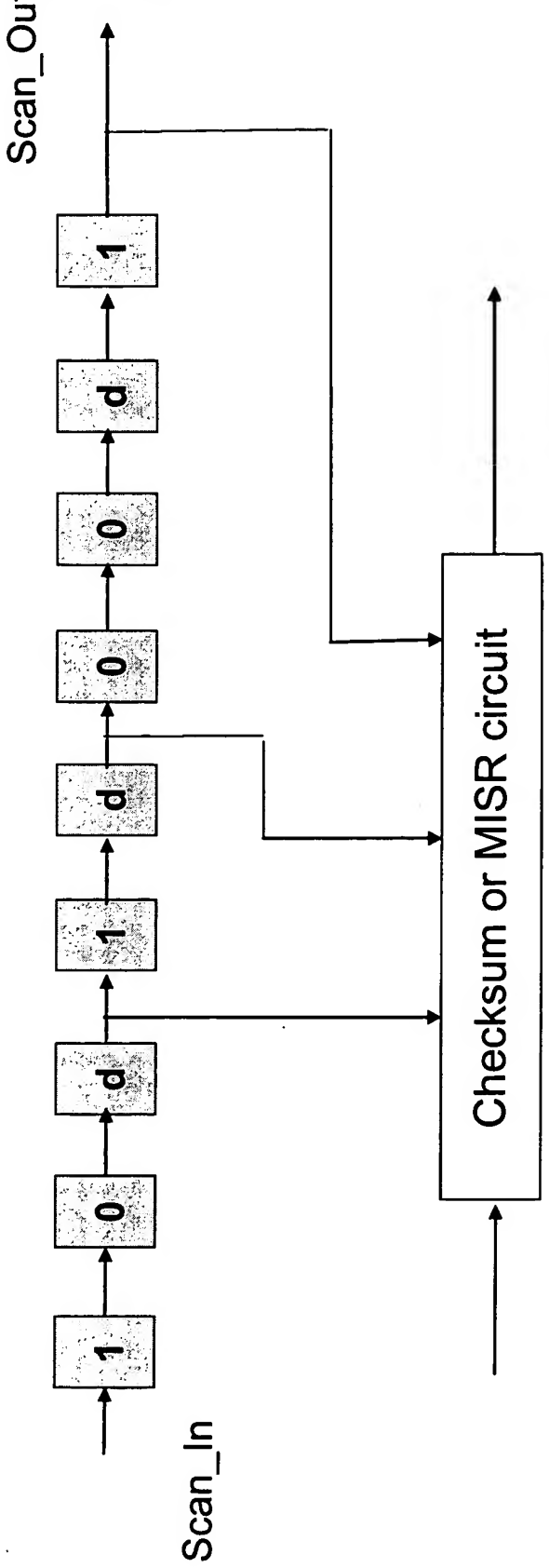
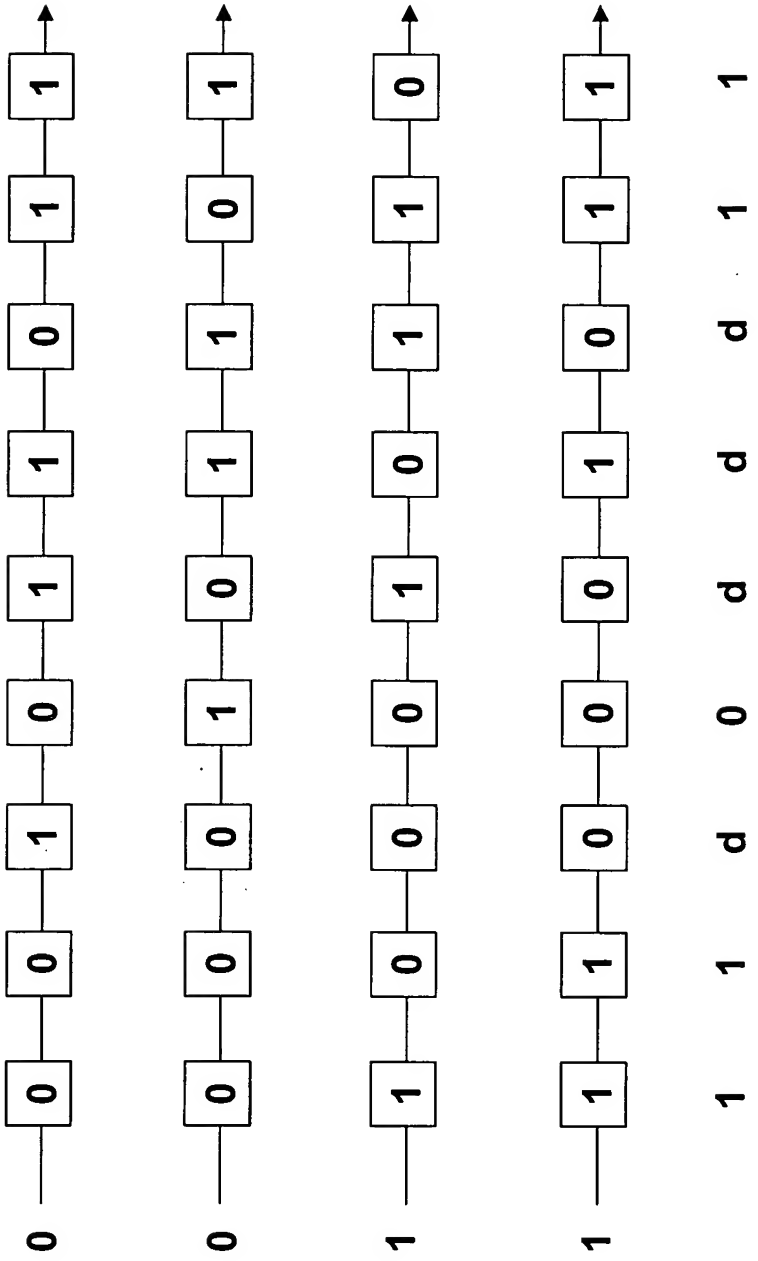


Figure 1


1 1 0 0 1 1 0 1 1 0 1 1 0 1 1 1

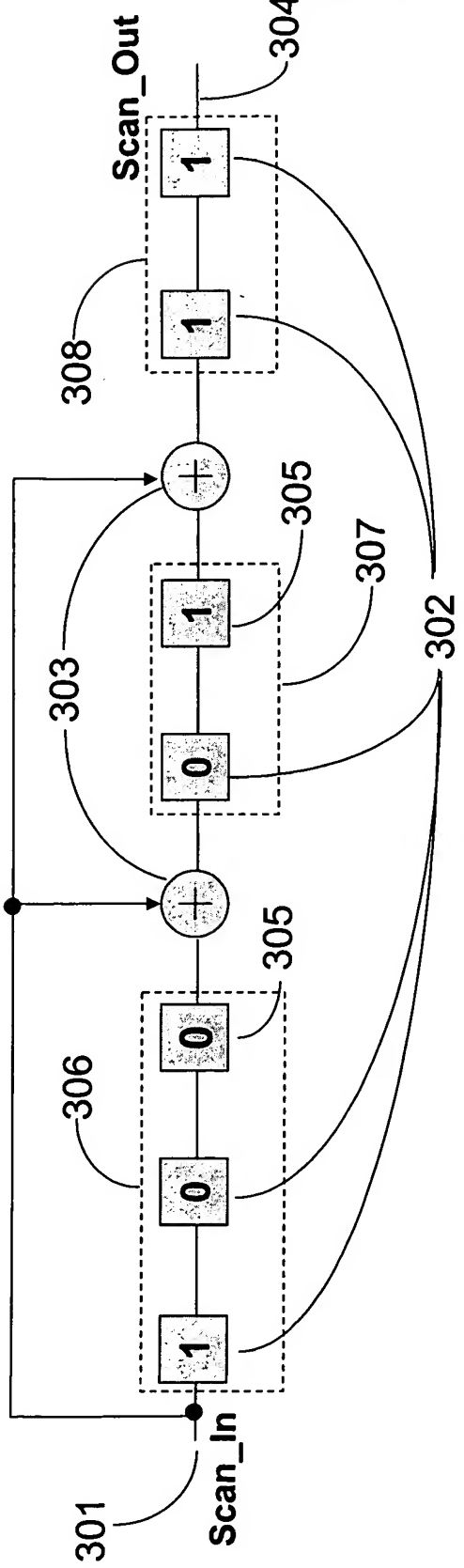


Figure 3

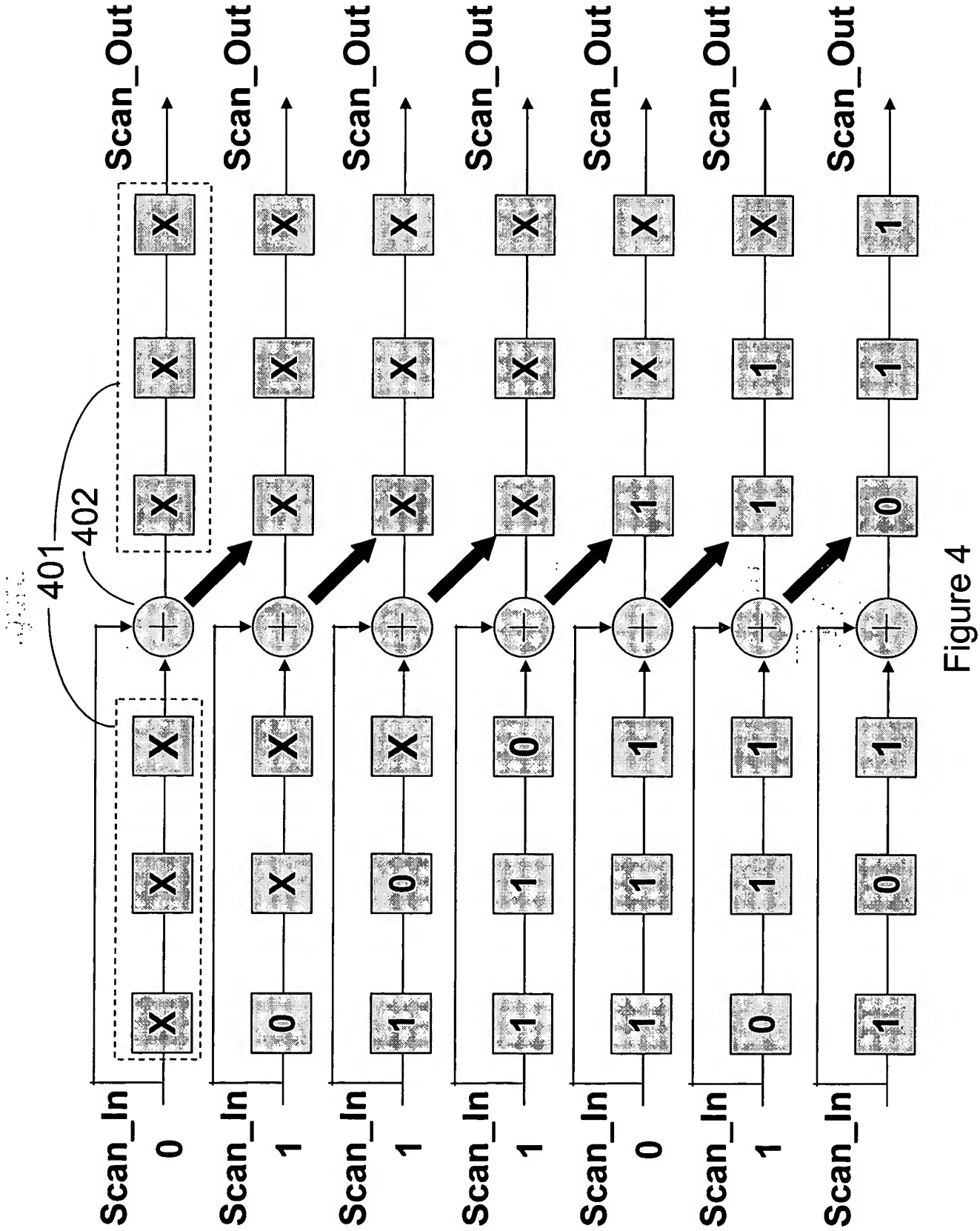


Figure 4

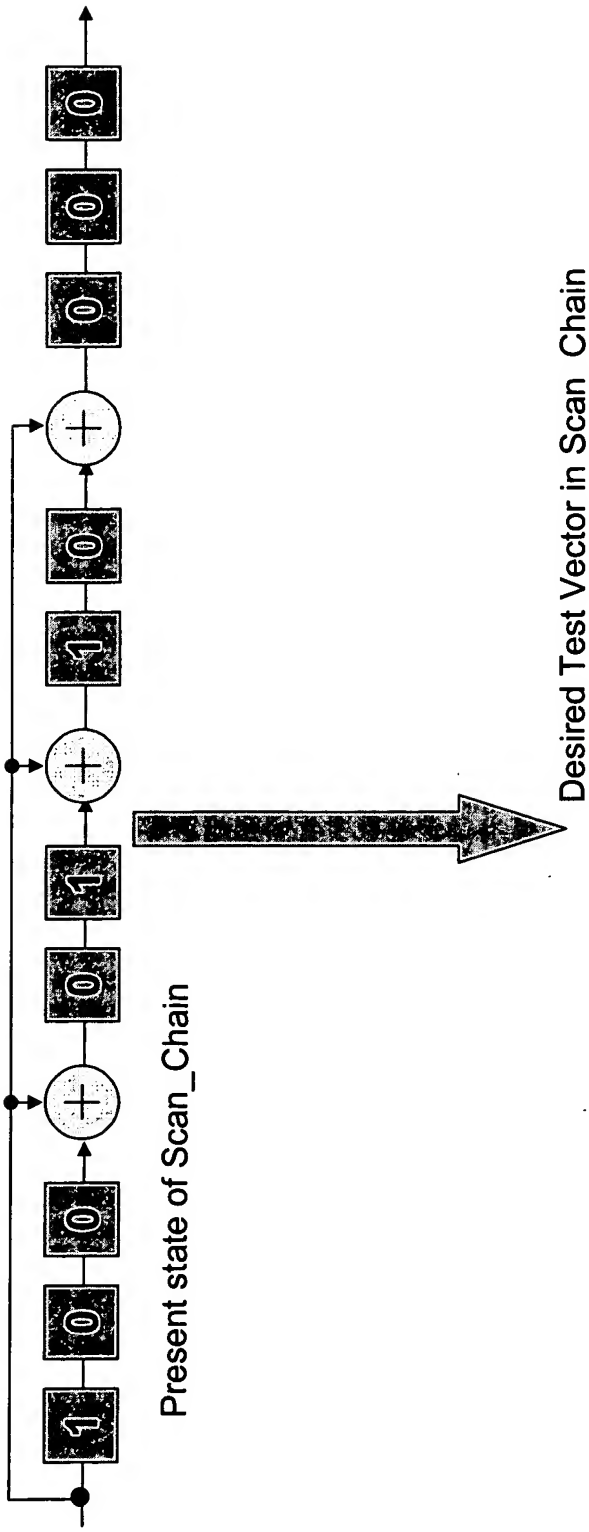

Present state of Scan_Chain
Desired Test Vector in Scan_Chain
1 d 1 0 d d 1 0 1 d

Figure 5a

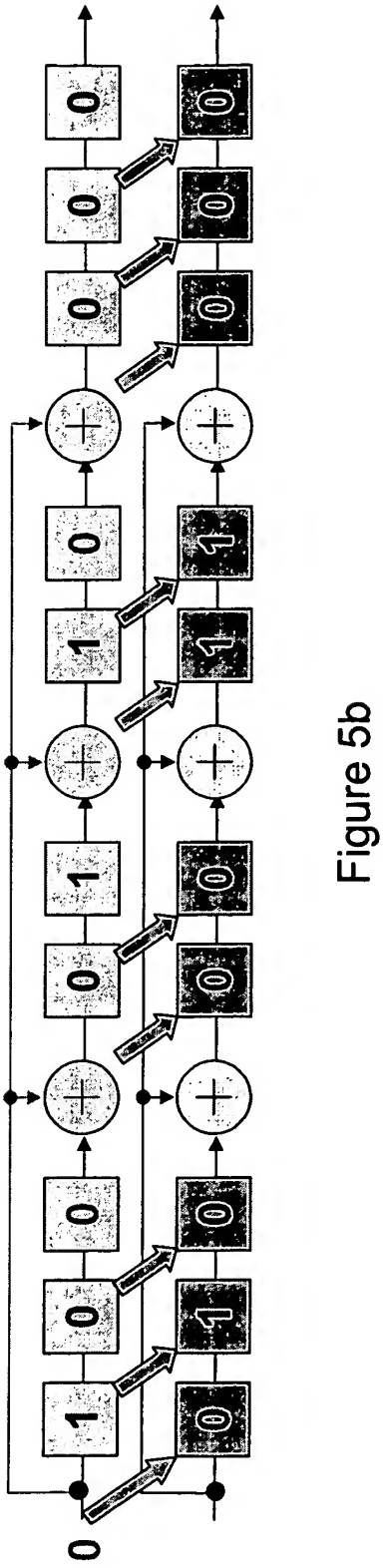


Figure 5b

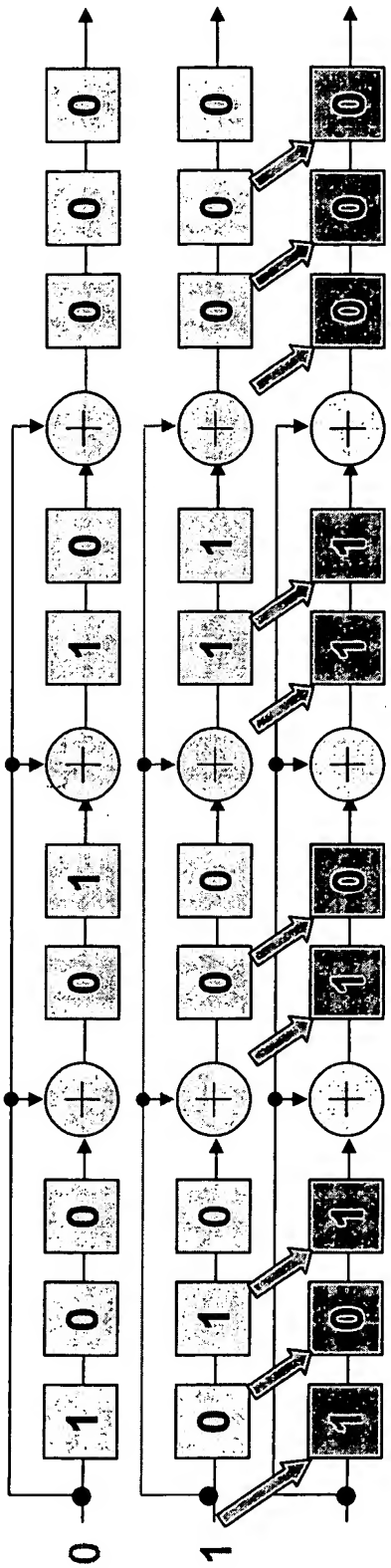


Figure 5c

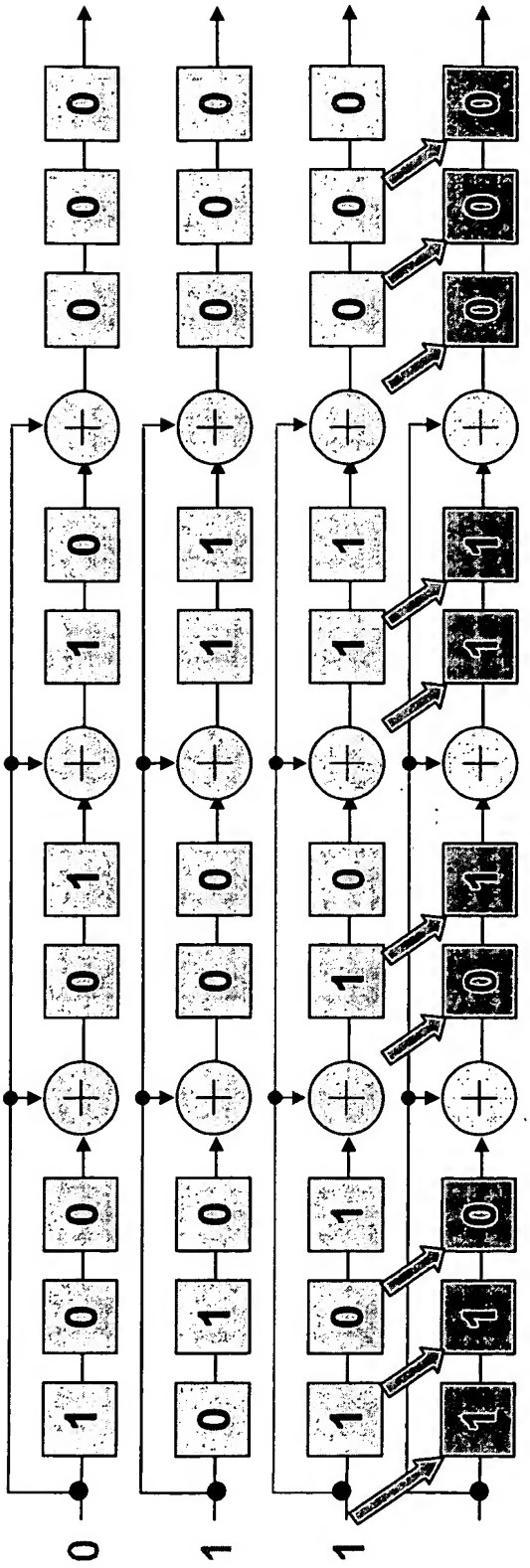


Figure 5d

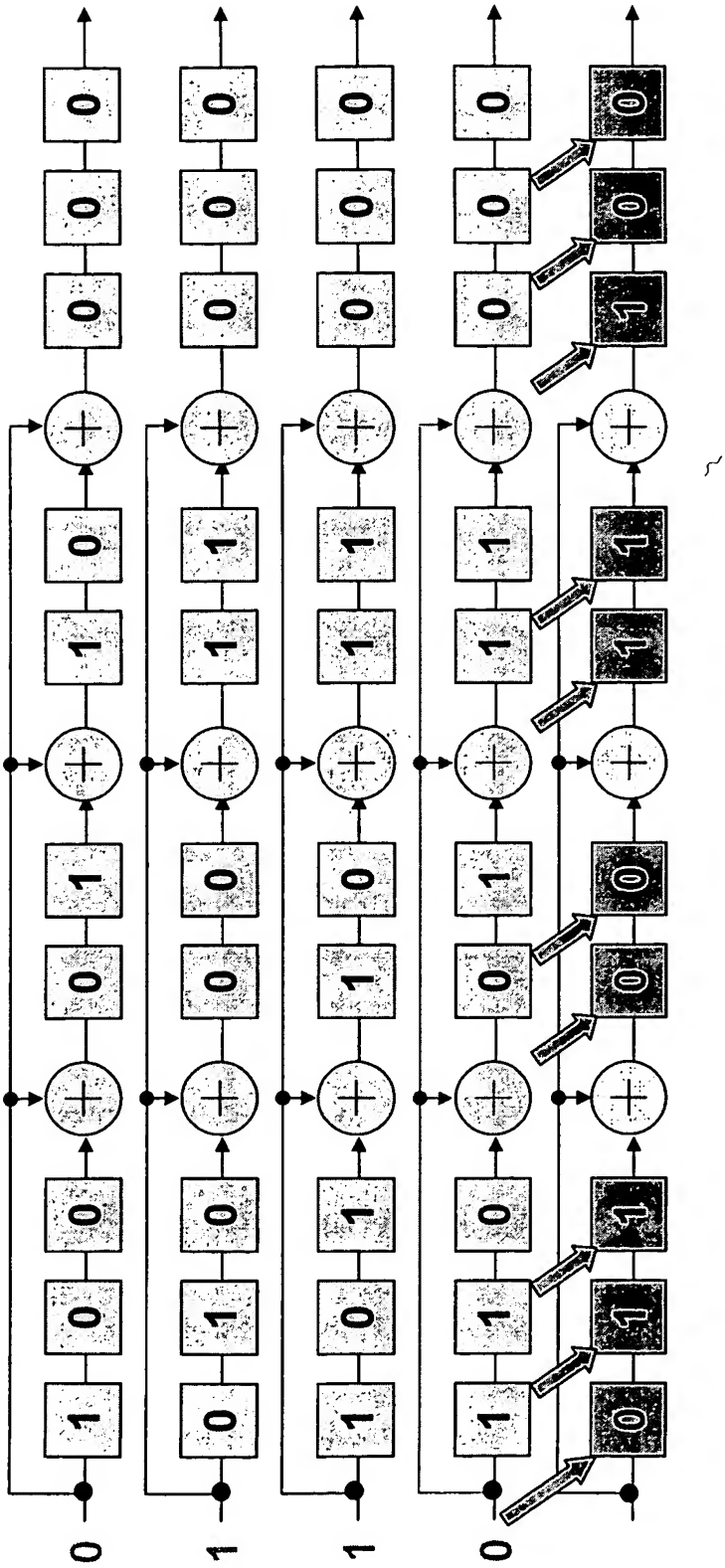


Figure 5e

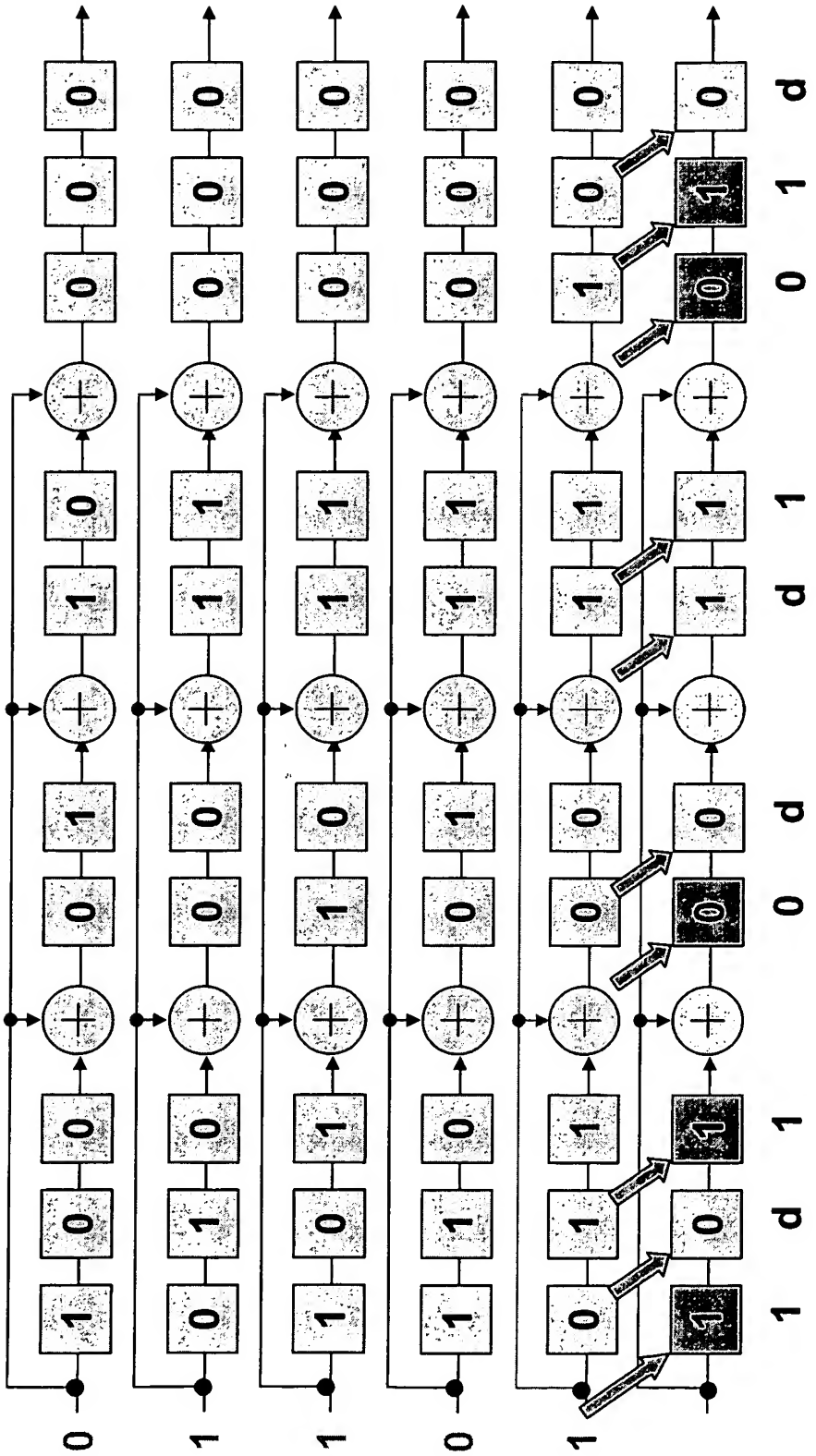


Figure 5f

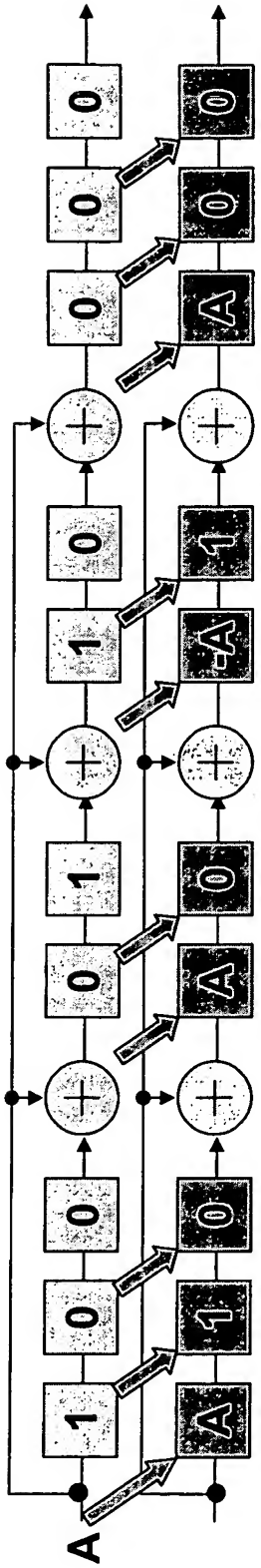


Figure 6a

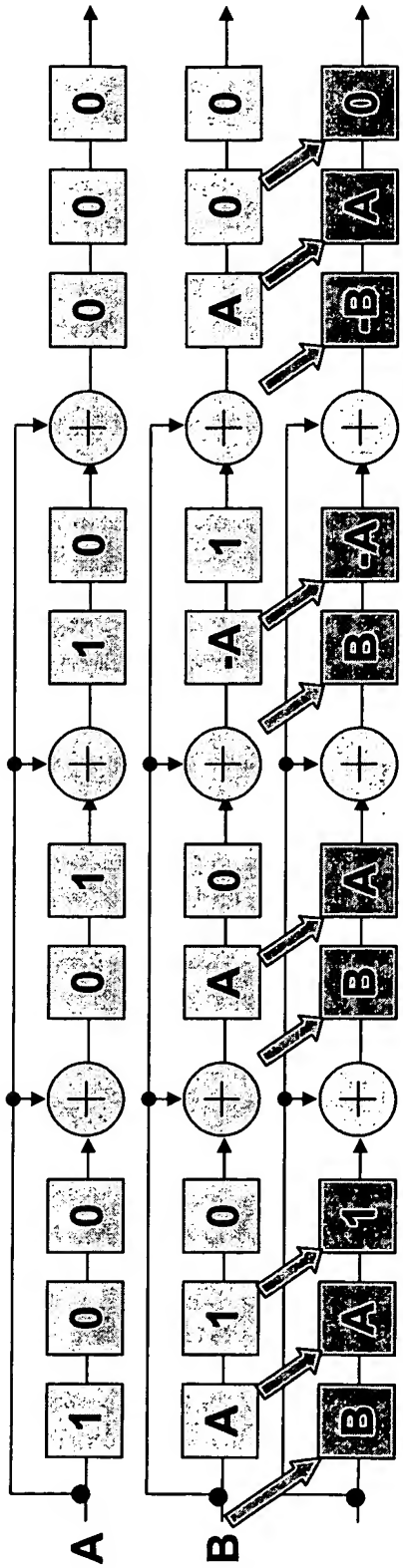


Figure 6b

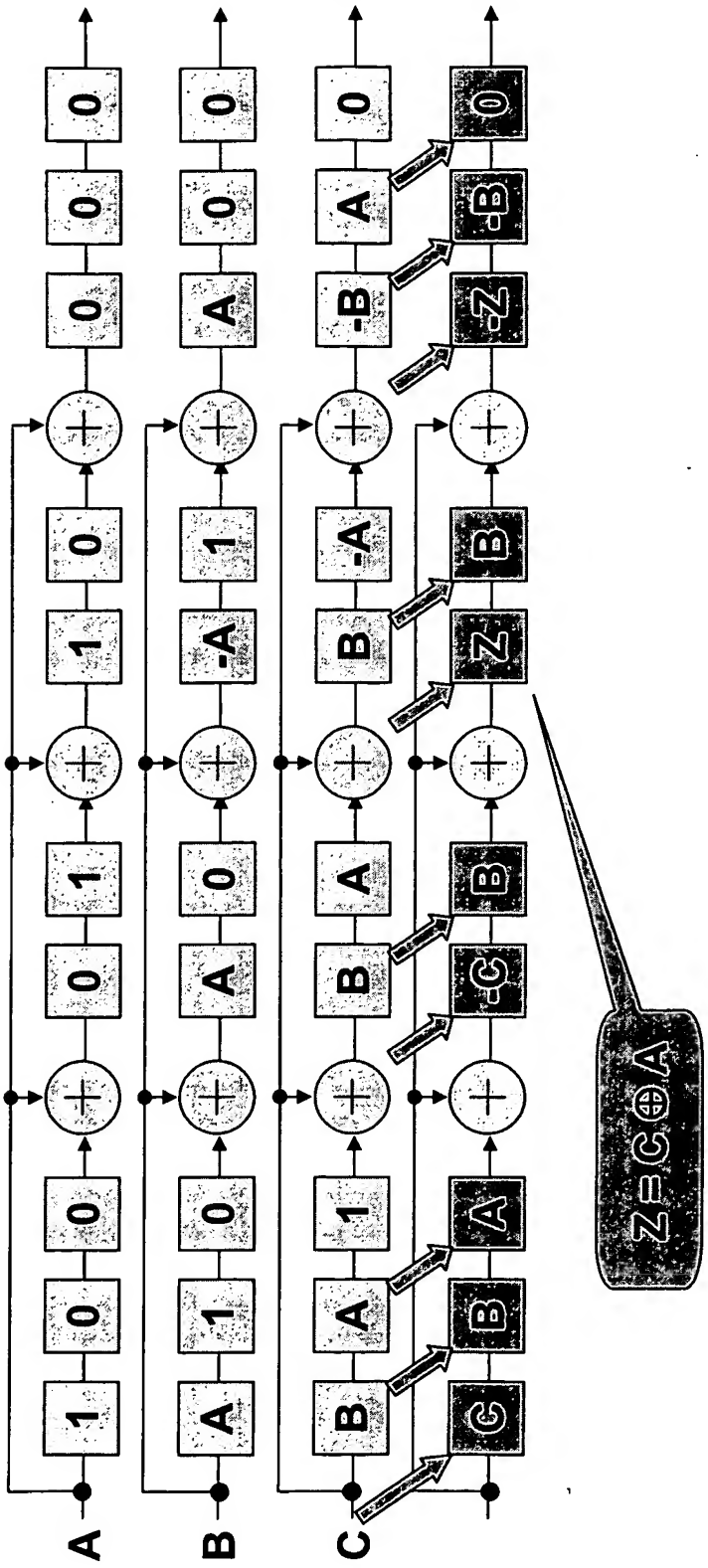


Figure 6c

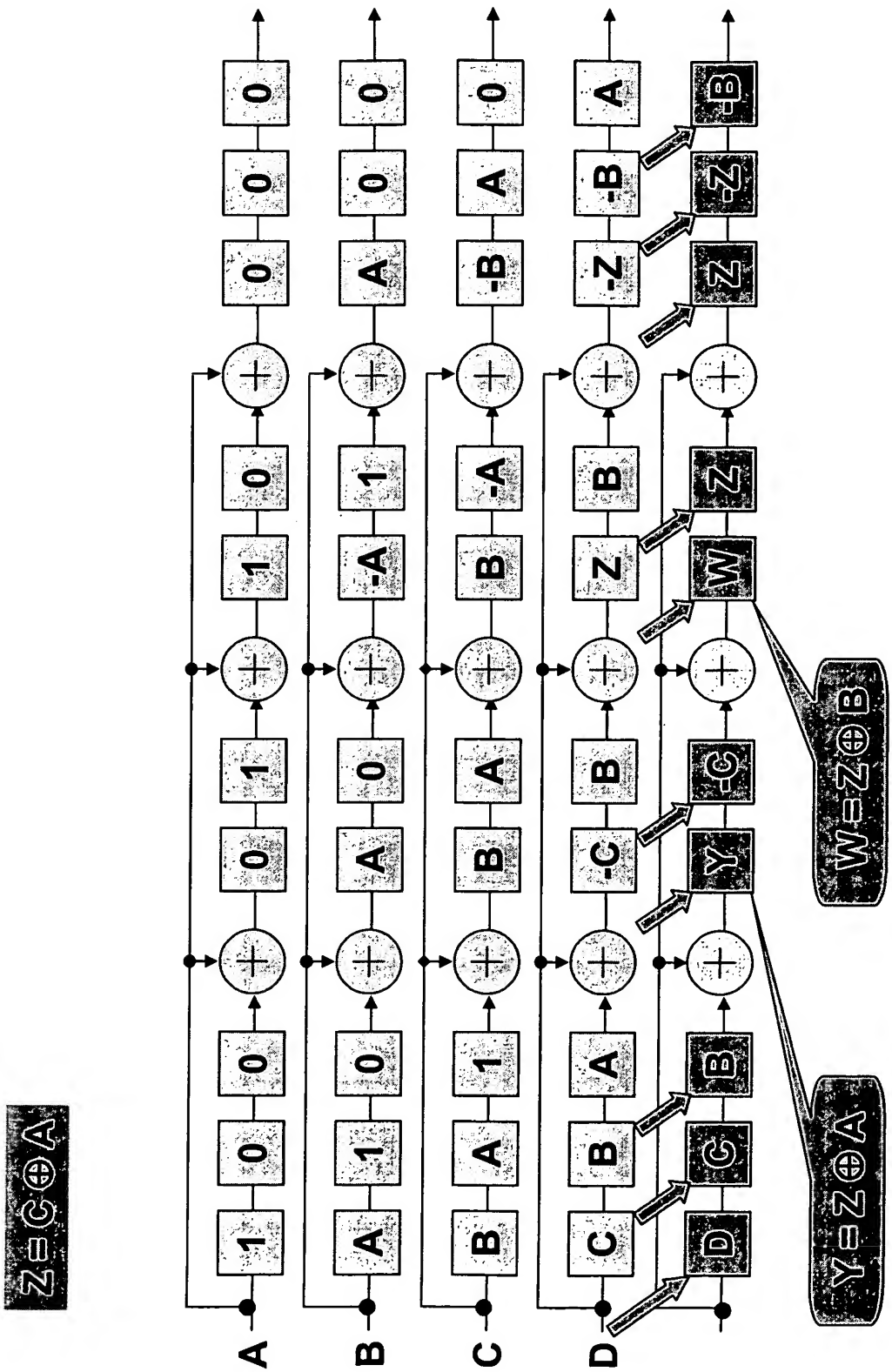


Figure 6d

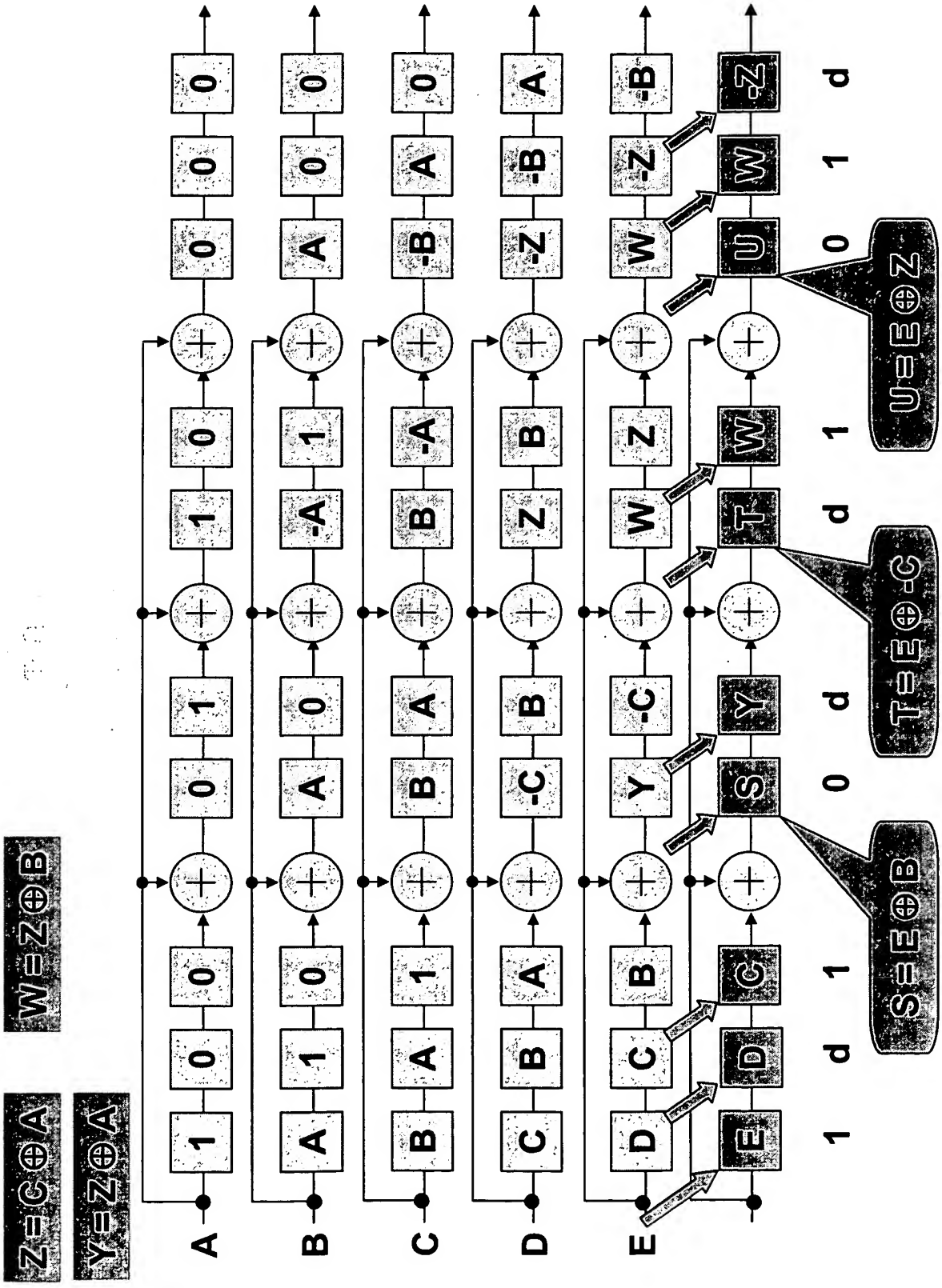


Figure 6e

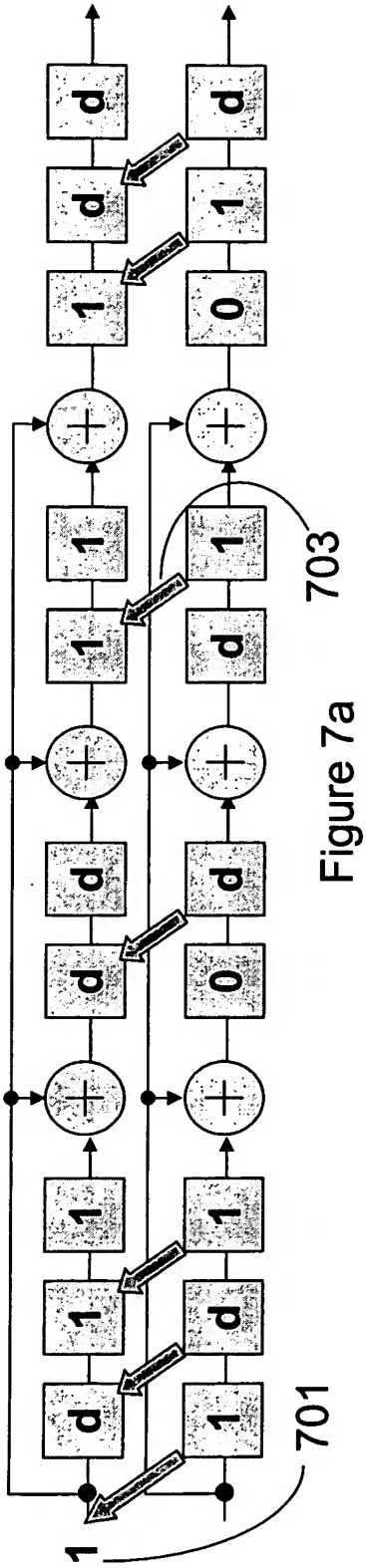


Figure 7a

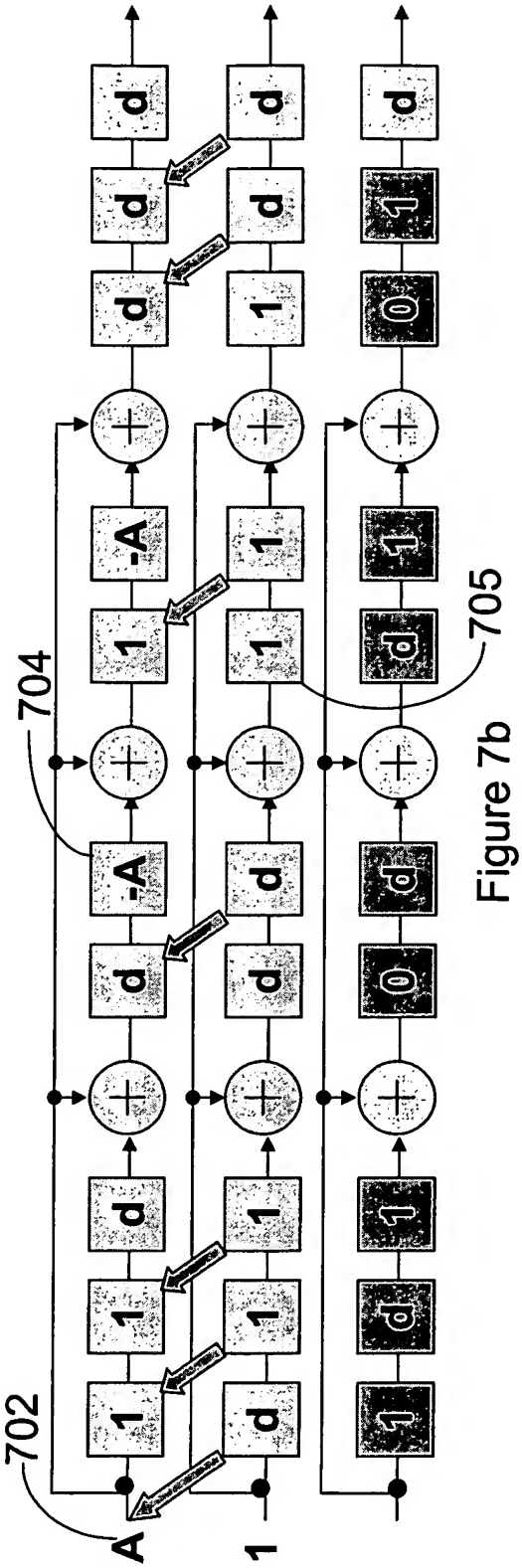


Figure 7b

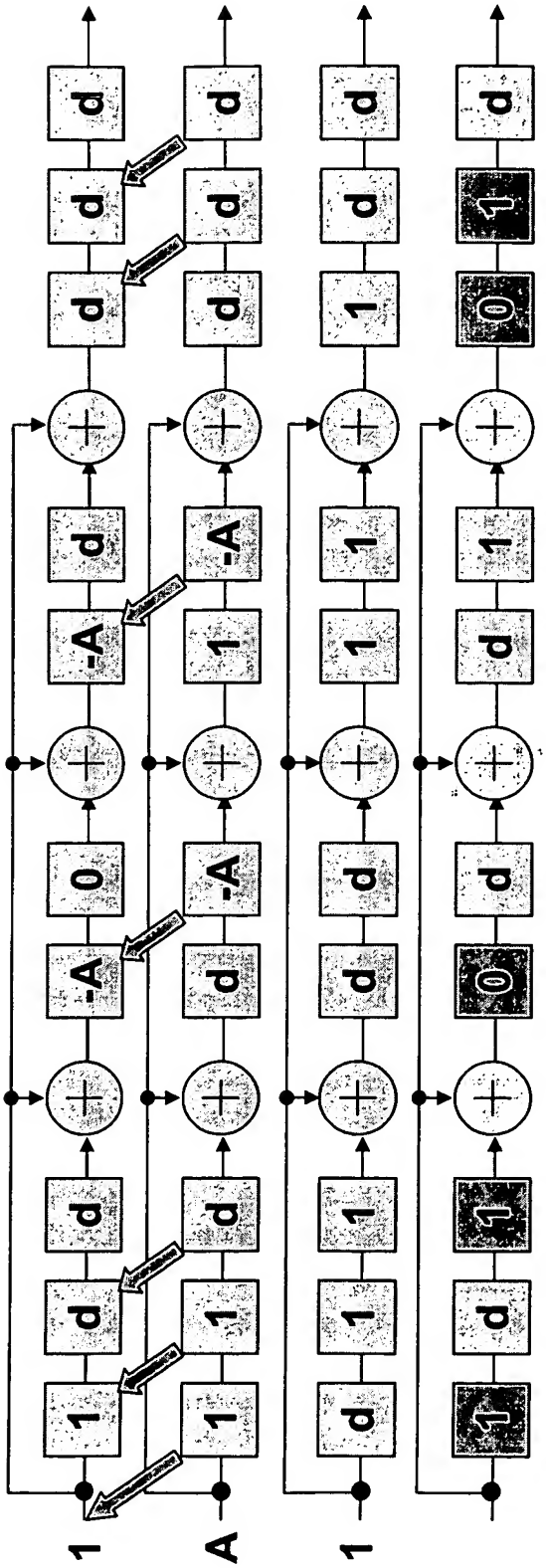


Figure 7c

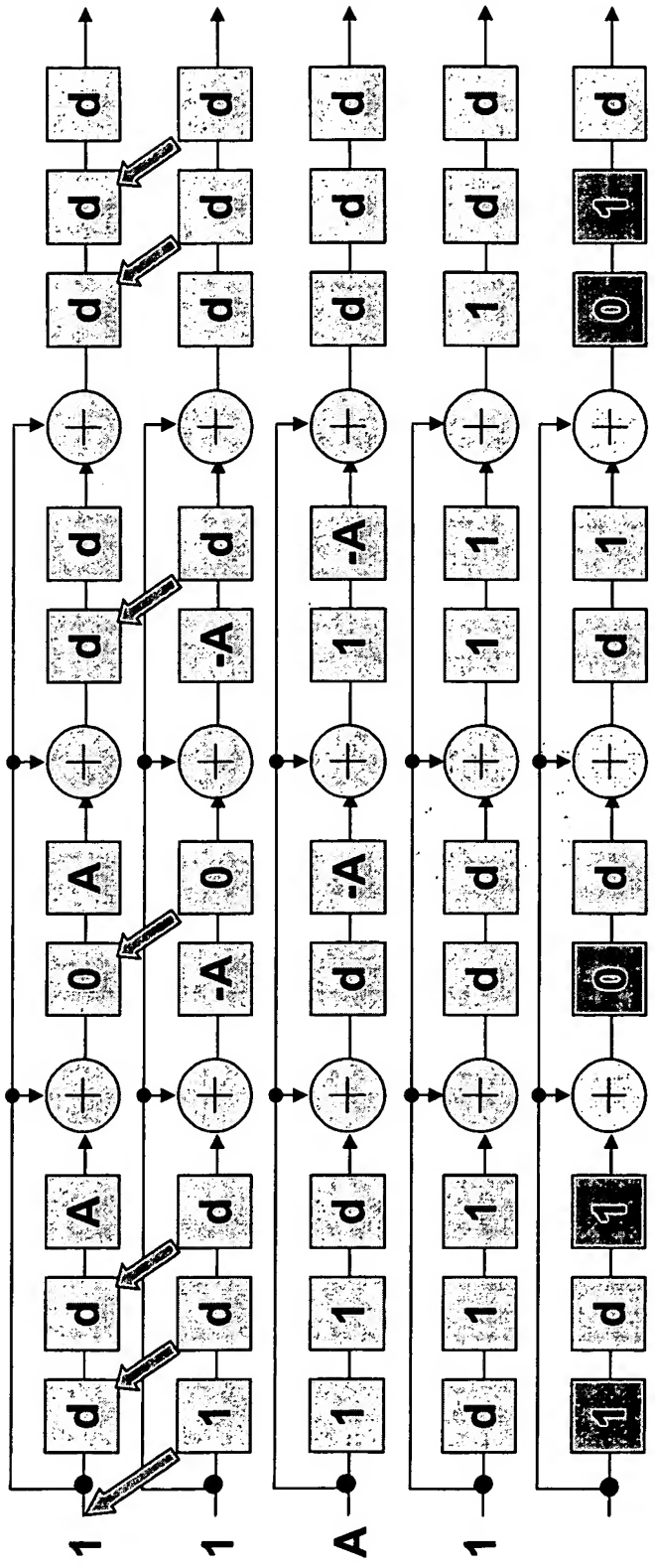


Figure 7d

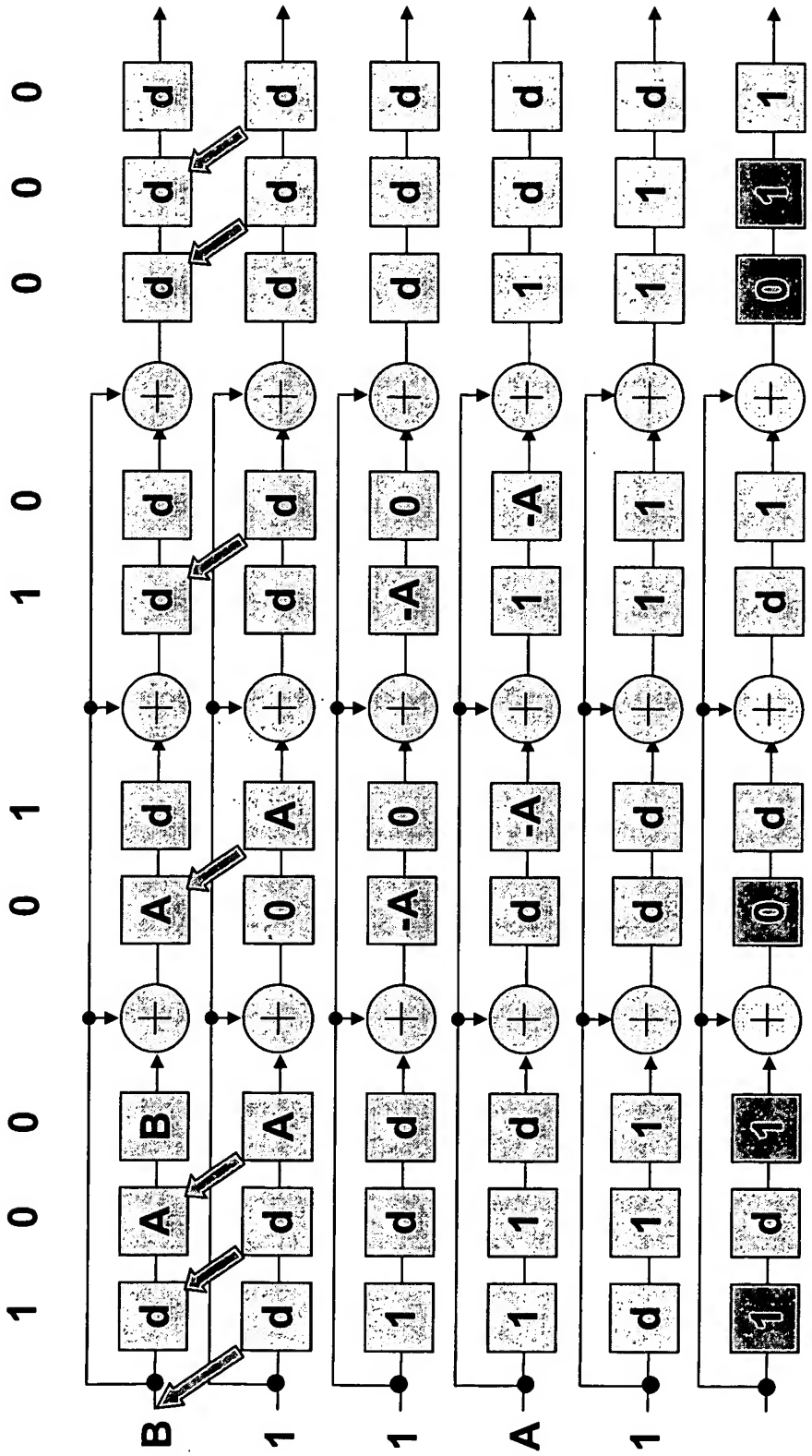


Figure 7e

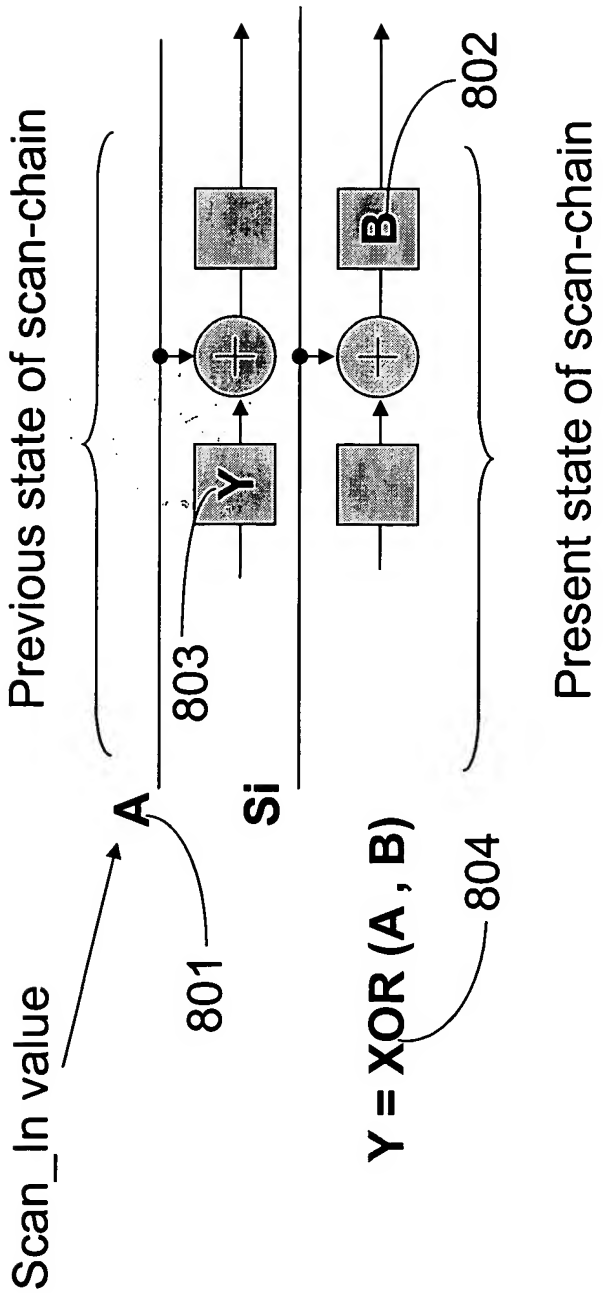

Scan_In value
A
801
803
Y
Si
B
802
Y = XOR (A , B)
804
Previous state of scan-chain
Present state of scan-chain

Figure 8

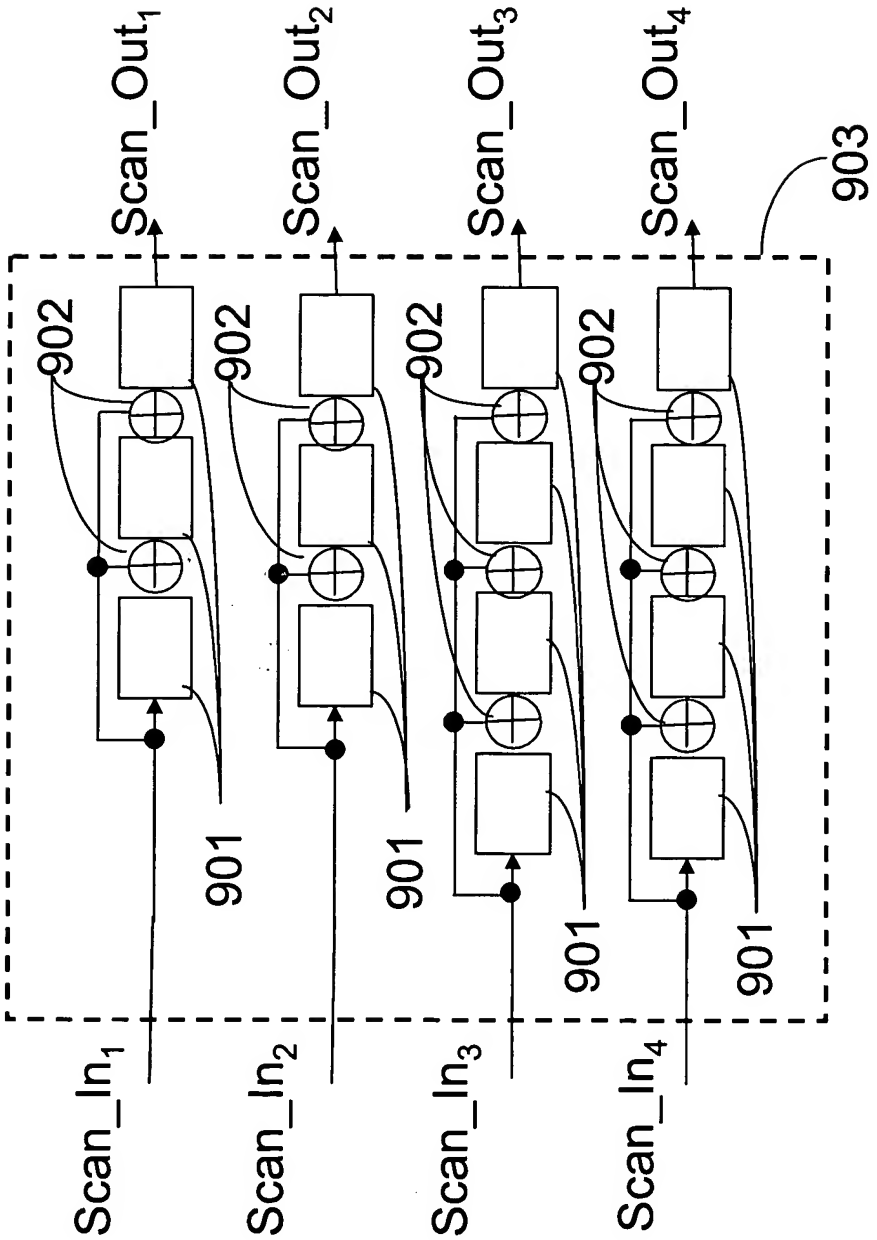

Scan_Out1
Scan_Out2
Scan_Out3
Scan_Out4
903
902
901
Scan_In1
Scan_In2
Scan_In3
Scan_In4

Figure 9

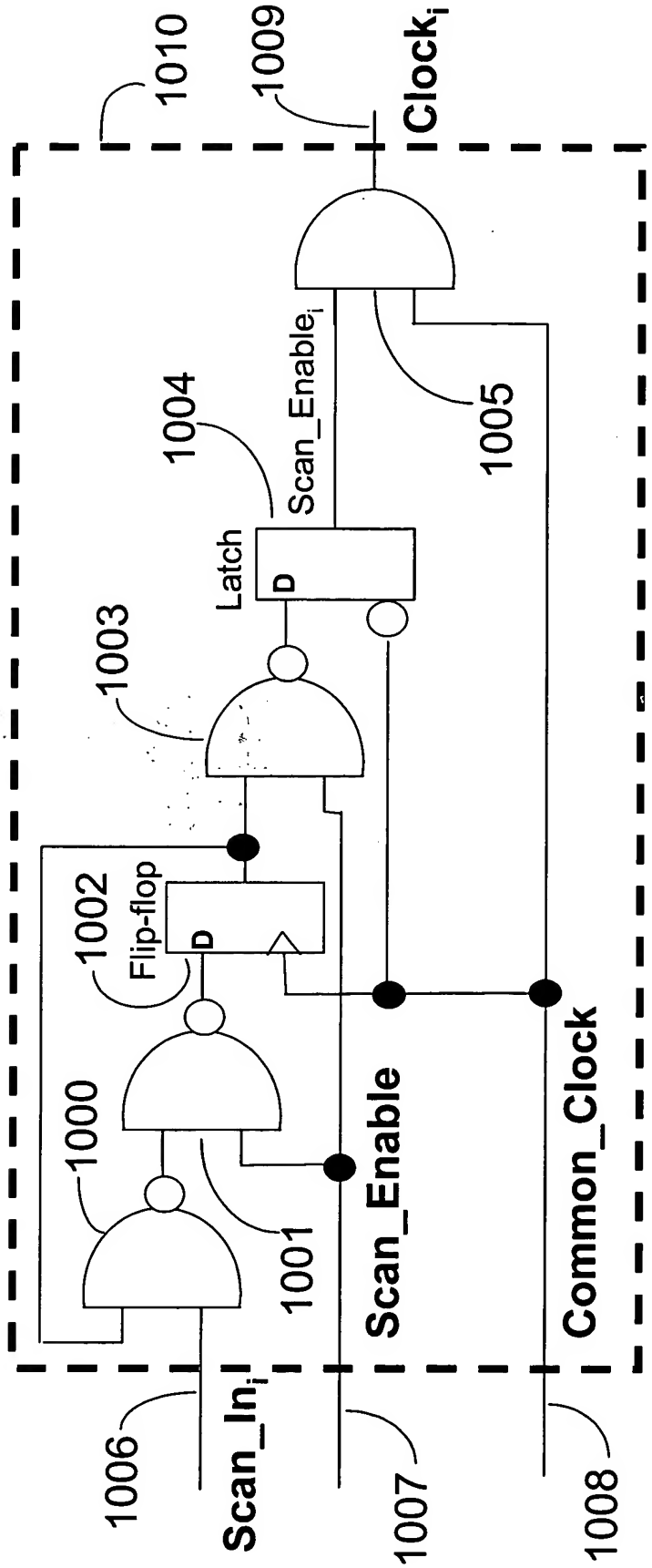

1010
1009
Clock$_i$
1004
Scan_Enable$_i$
1005
Latch
D
1003
1002
Flip-flop
D
1000
1001
Scan_Enable
Common_Clock
1006
Scan_In$_i$
1007
1008

Figure 10a

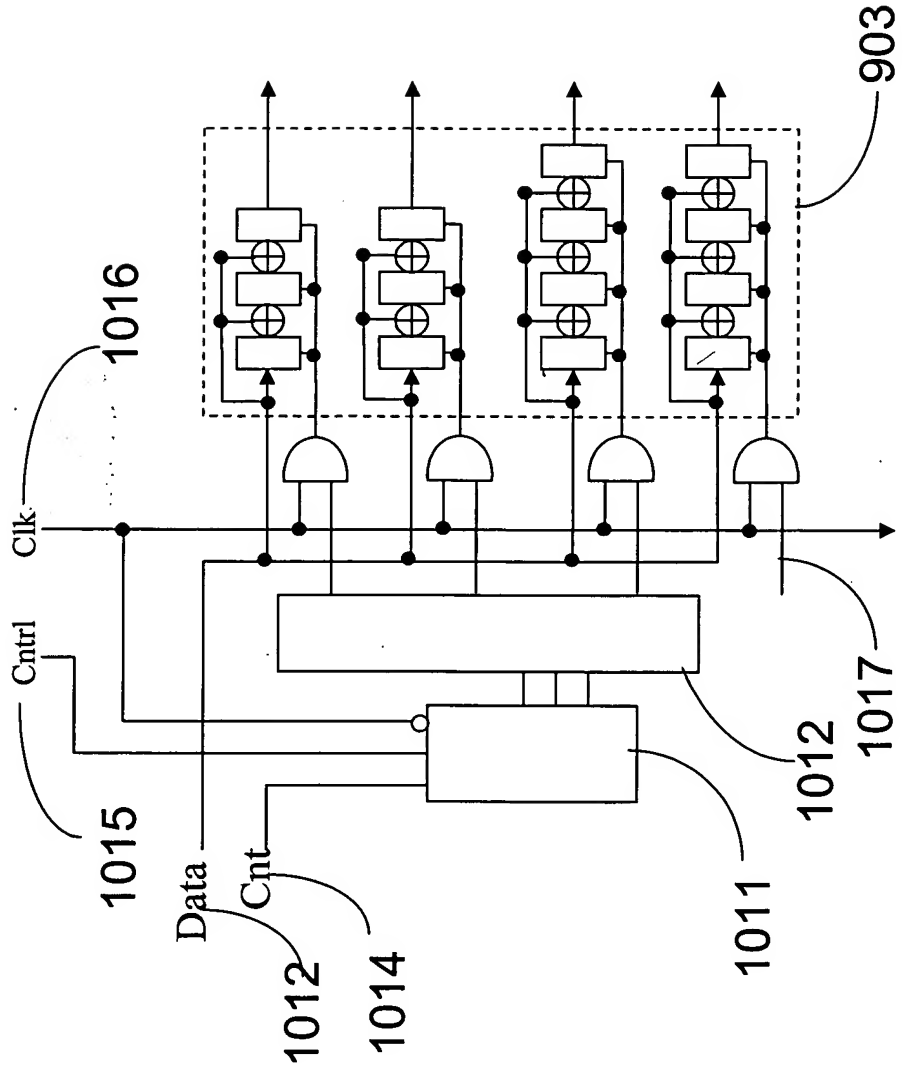


Figure 10b

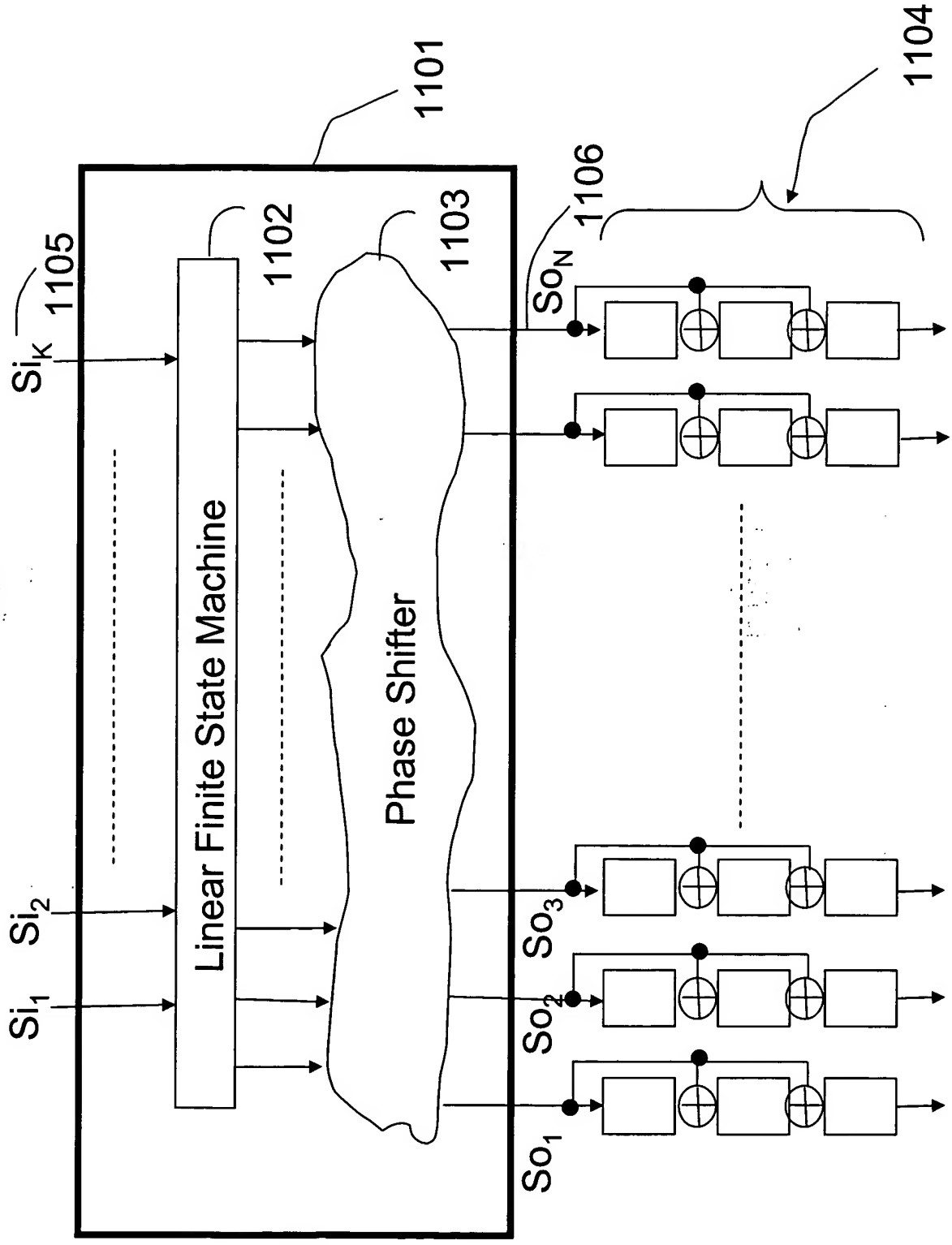

1101
1104
1105
1102
1103
1106
Si_K
Si_2
Si_1
So_N
So_3
So_2
So_1
Linear Finite State Machine
Phase Shifter

Figure 11

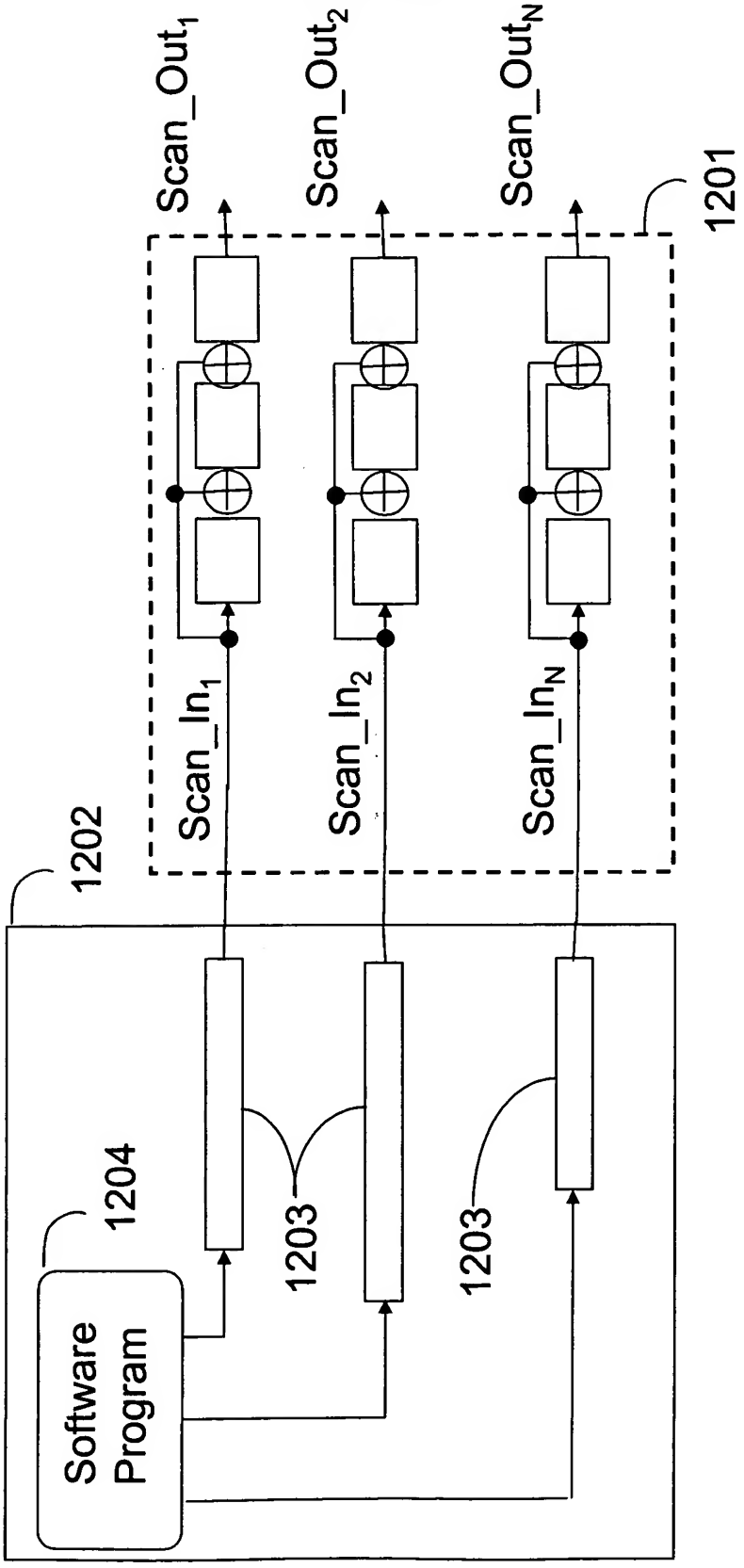

Scan_Out1
Scan_Out2
ScanOutN
1201
Scan_In1
Scan_In2
Scan_InN
1202
1203
1203
1204
Software Program

Figure 12

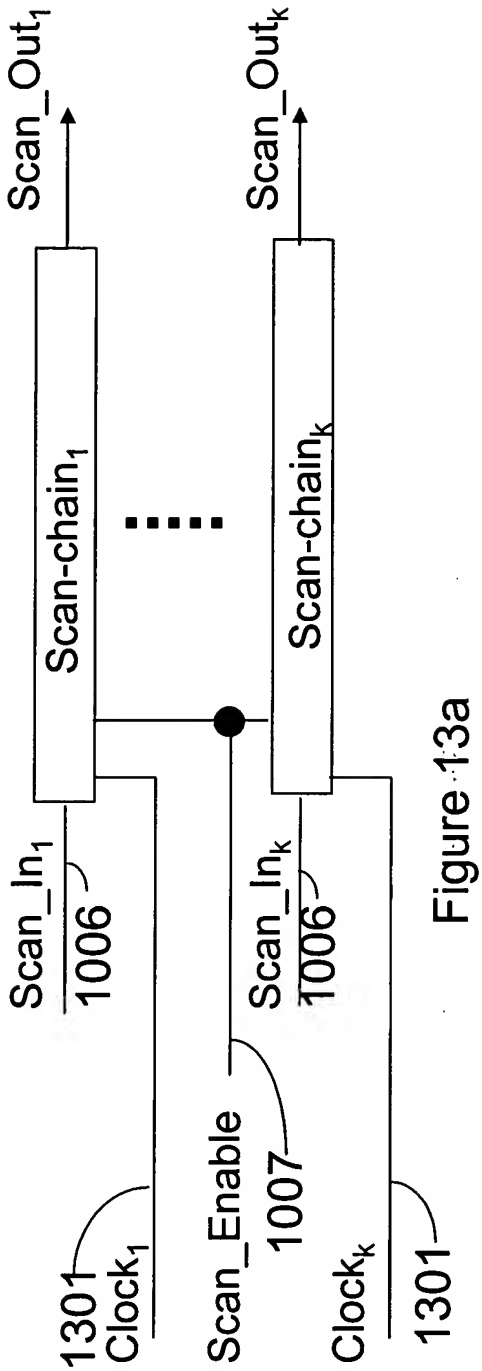


Figure 13a

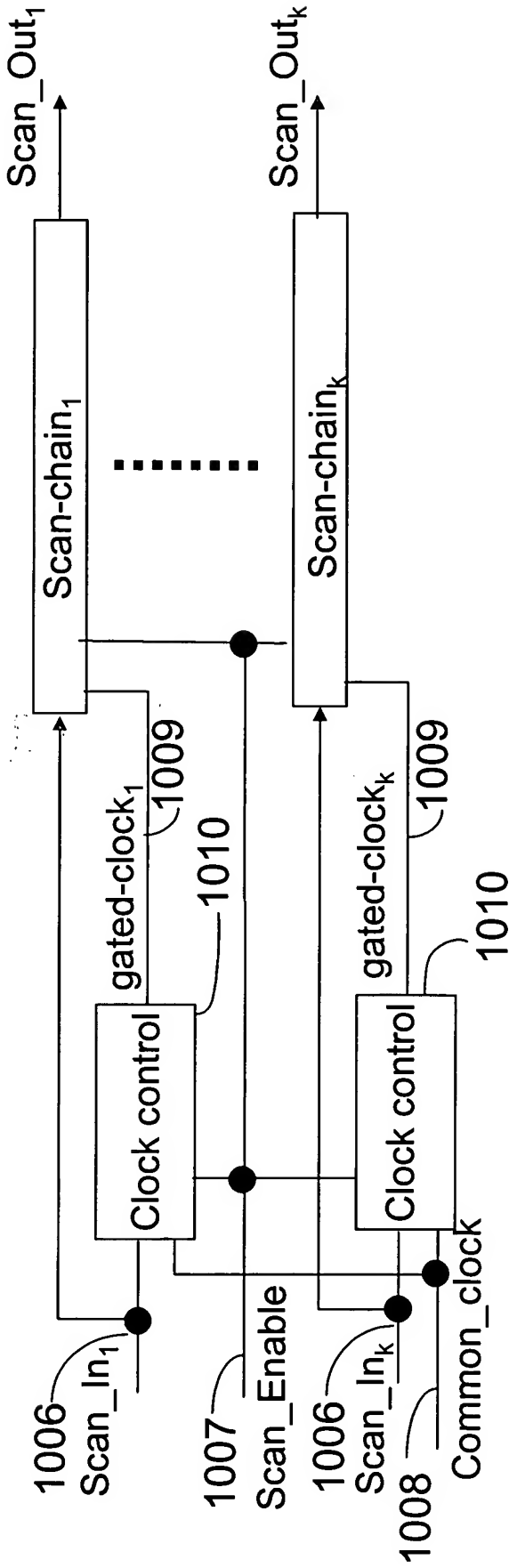


Figure 13b

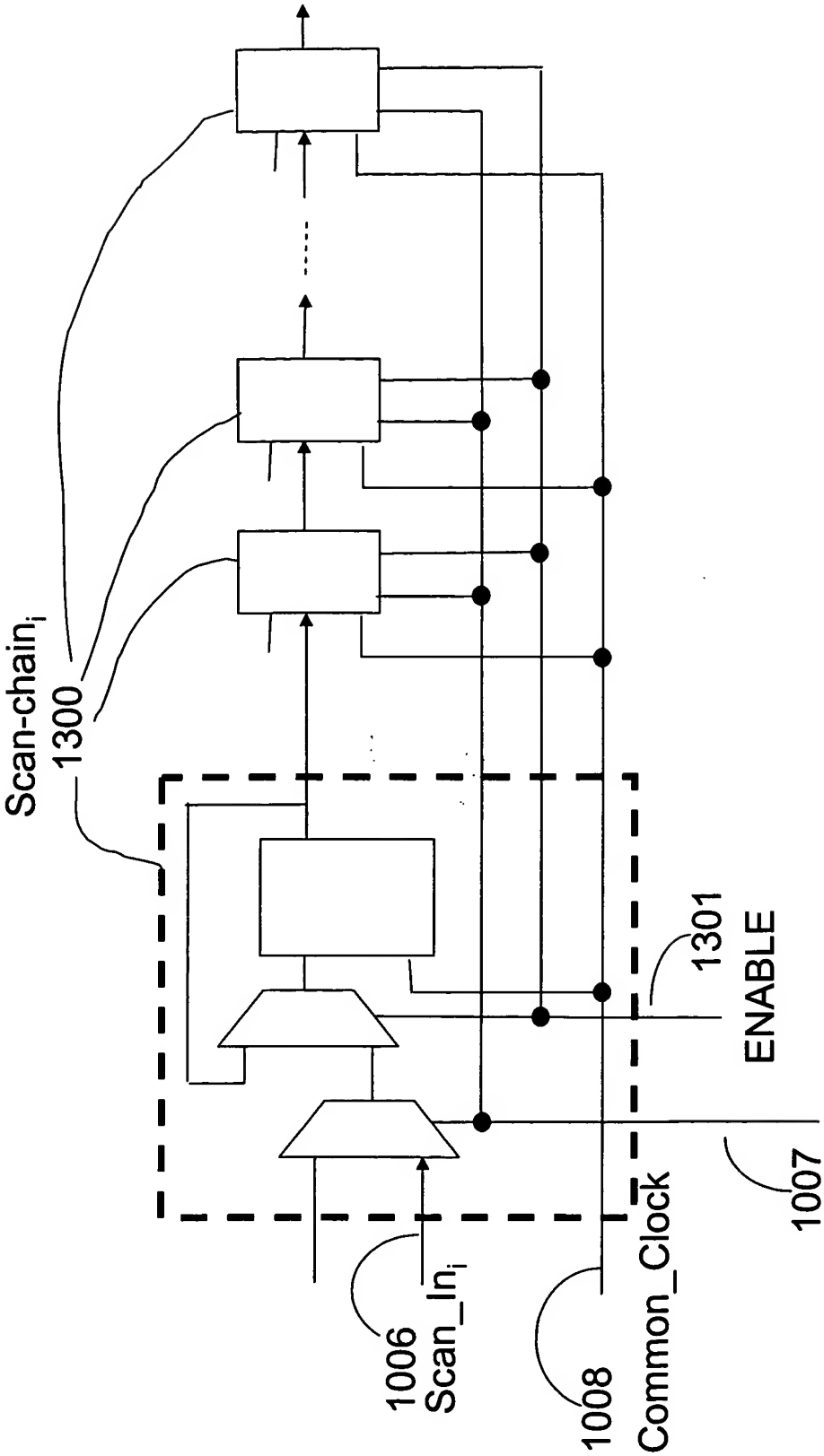

Scan-chain$_i$
1300
1301
ENABLE
Scan_Enable
1007
Common_Clock
1008
Scan_In$_i$
1006

Figure 13c

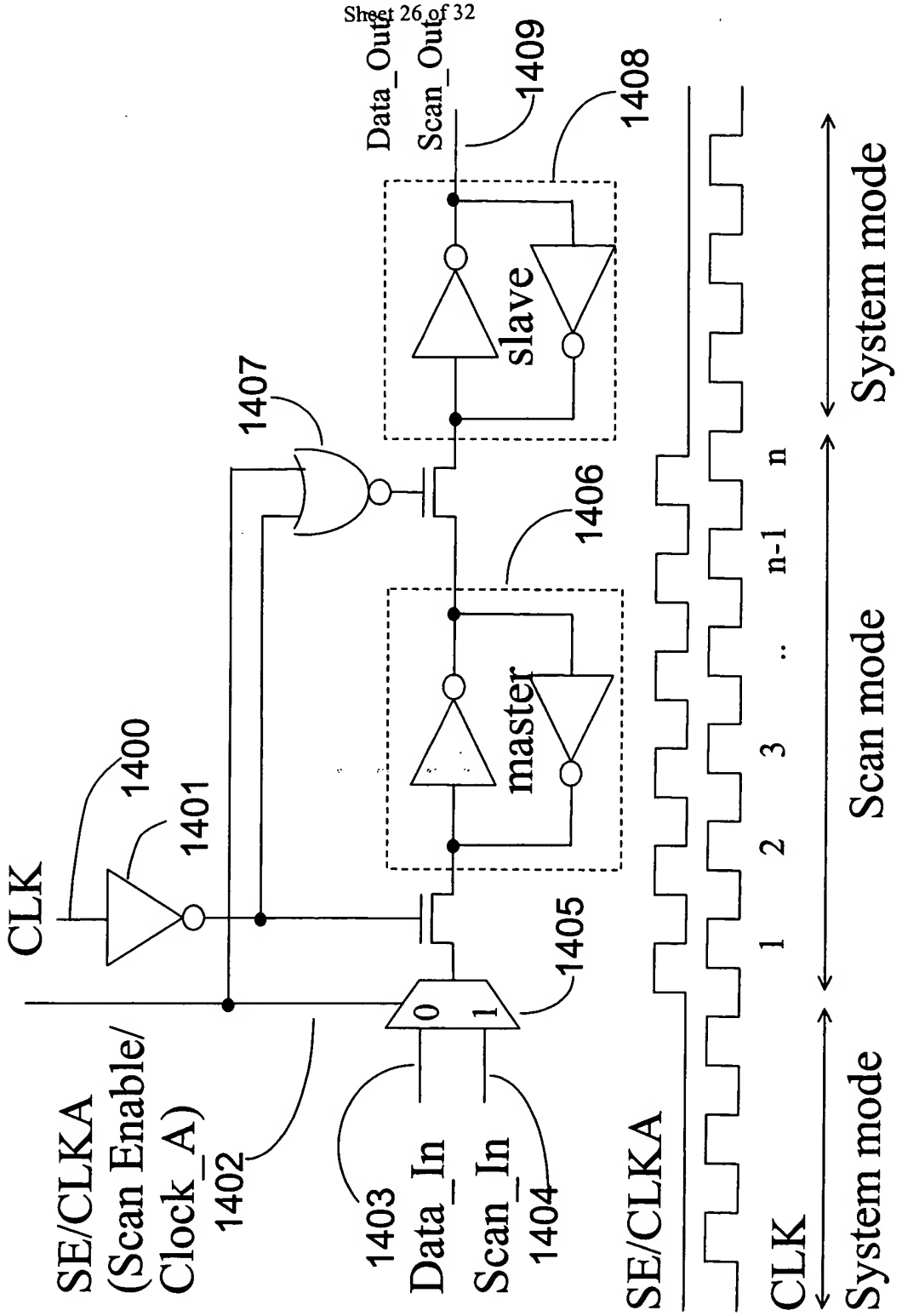

CLK
1400
1401
SE/CLKA
(Scan Enable/
Clock_A)
1402
1403
Data_In
Scan_In
1404
1405
0
1
master
1406
1407
slave
1408
1409
Data_Out
Scan_Out
SE/CLKA
CLK
1
2
3
..
n-1
n
Scan mode
System mode
System mode

Figure 14

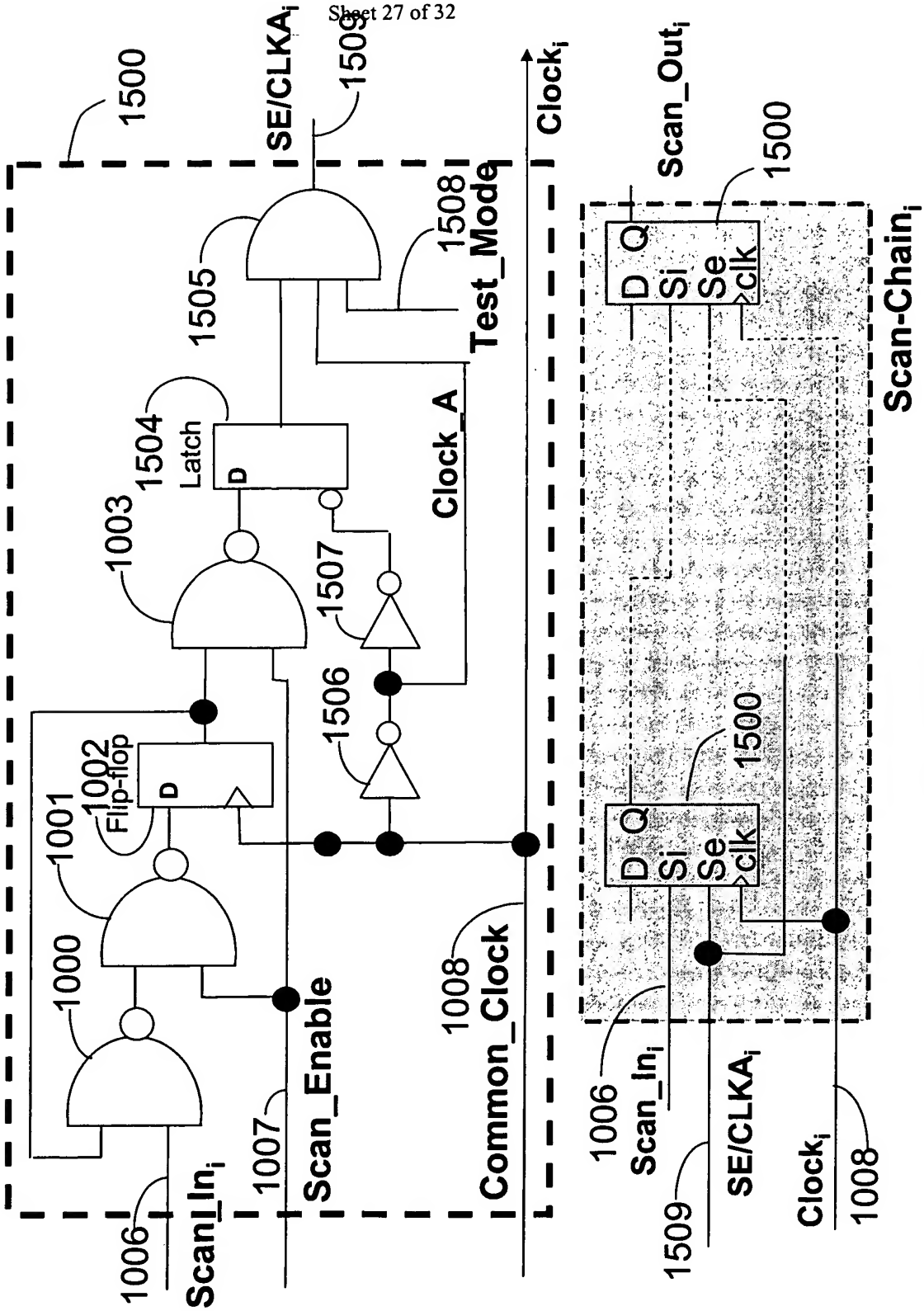

1500
SE/CLKA$_i$
1509
Clock$_i$
Scan_Out$_i$
1500
1505
1508
Test_Mode
1504
Latch
D
Clock_A
1003
1507
1506
1002
Flip-flop
D
1001
1000
Scan_Enable
1007
Common_Clock
1008
1006
Scan_In$_i$
1006
Scan_In$_i$
1509
SE/CLKA$_i$
Clock$_i$
1008
D Q
Si
Se
clk
1500
Scan-Chain$_i$

Figure 15a

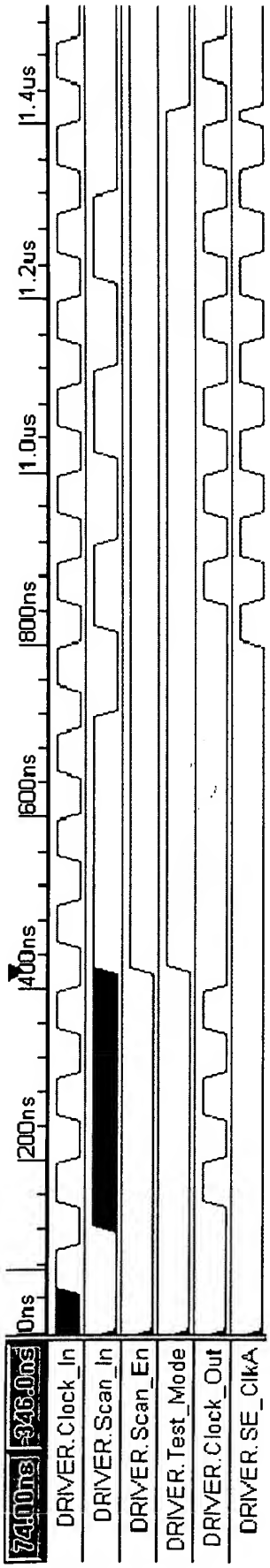

7400ns
-346.0ns
0ns
200ns
400ns
600ns
800ns
1.0us
1.2us
1.4us
DRIVER.Clock_In
DRIVER.Scan_In
DRIVER.Scan_En
DRIVER.Test_Mode
DRIVER.Clock_Out
DRIVER.SE_ClkA

Figure 15b

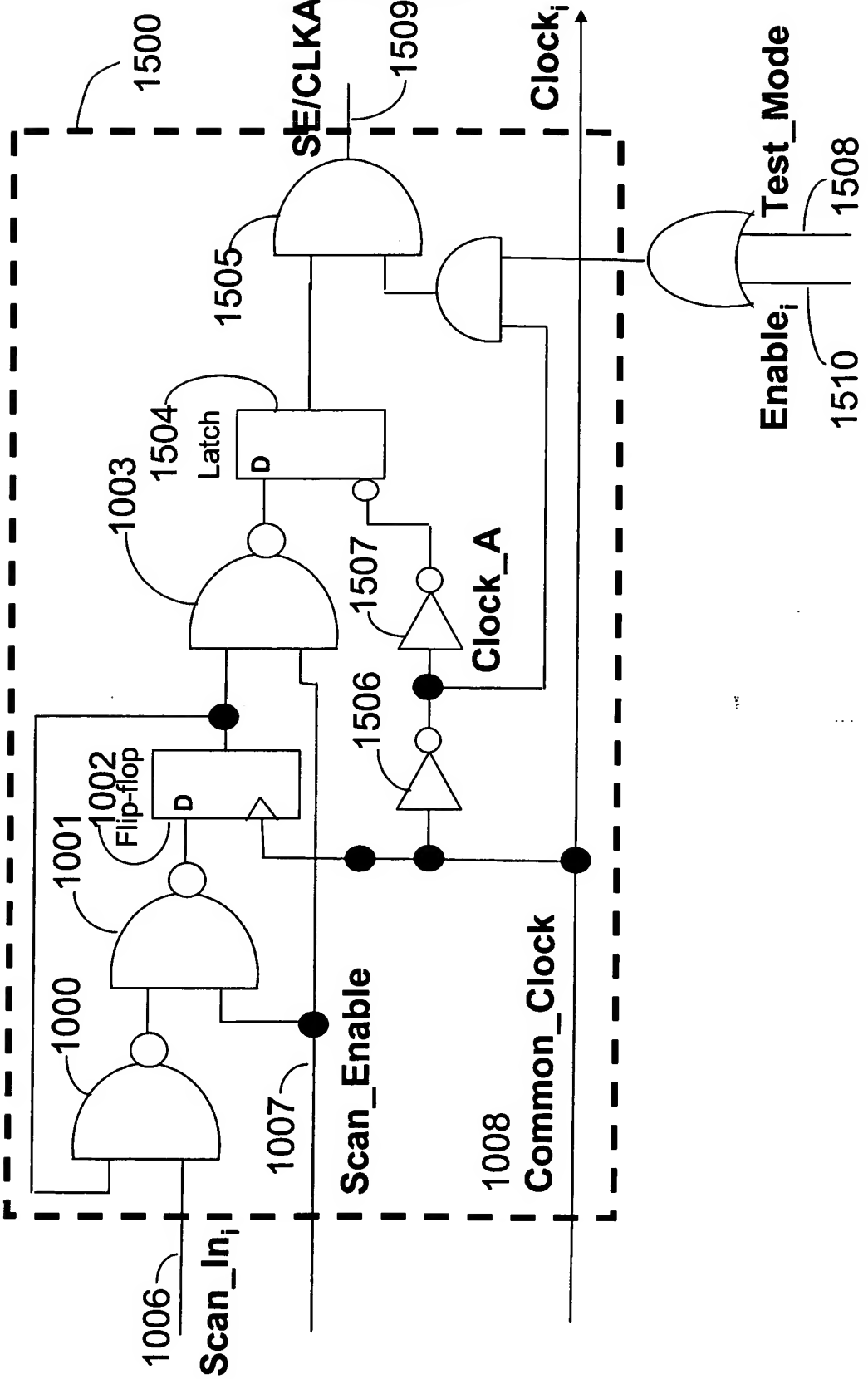

1500
SE/CLKA$_i$
1509
Clock$_i$
Test_Mode
1508
1505
1504
Latch
D
Enable$_i$
1510
1003
1507
Clock_A
1506
1002
Flip-flop
D
1001
1000
1007
Scan_Enable
1008
Common_Clock
1006
Scan_In$_i$

Figure 15c

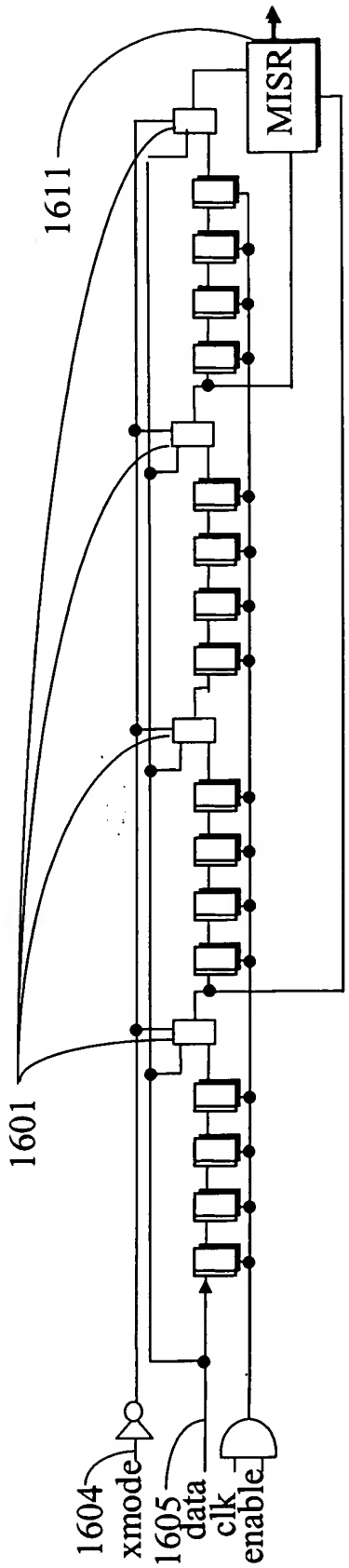


Figure 16a

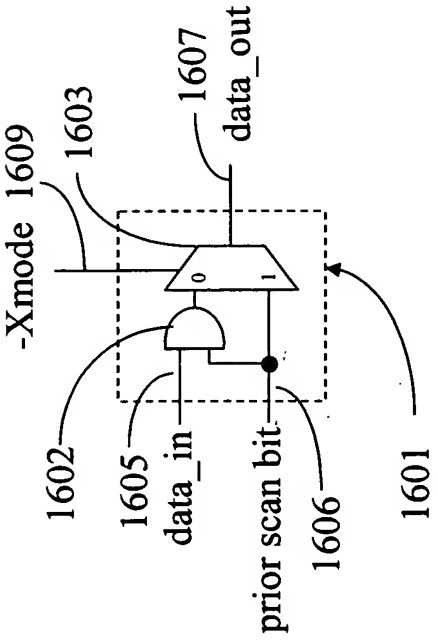


Figure 16b

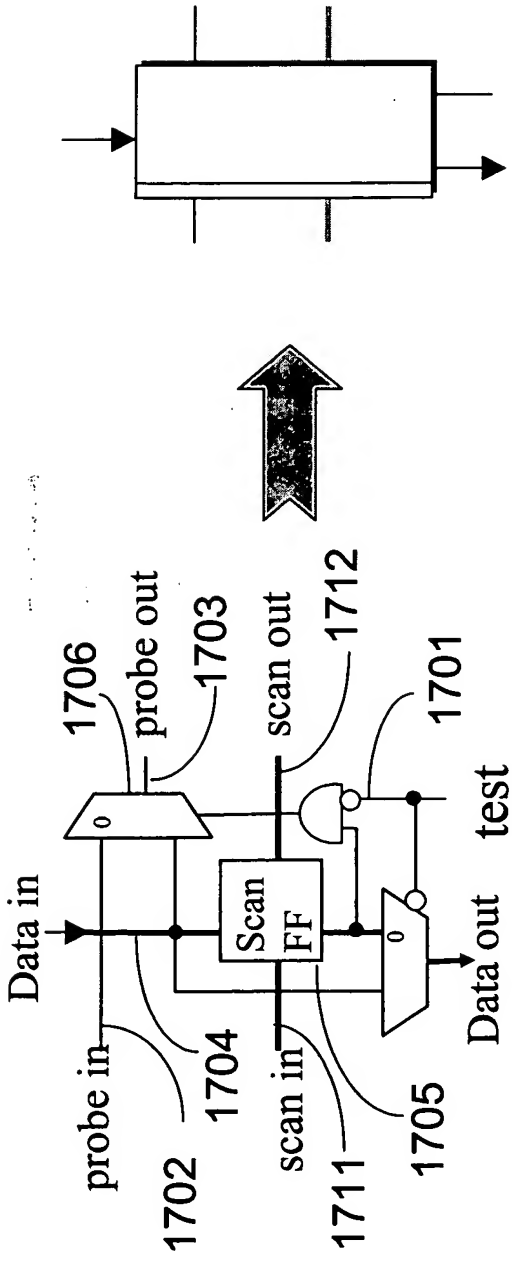


Figure 17a

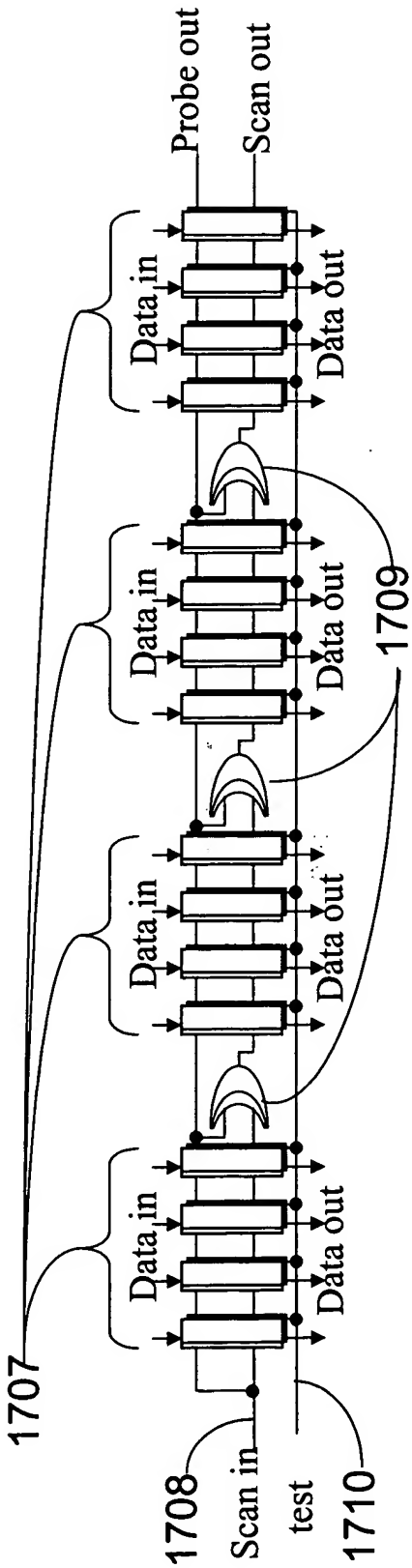


Figure 17b

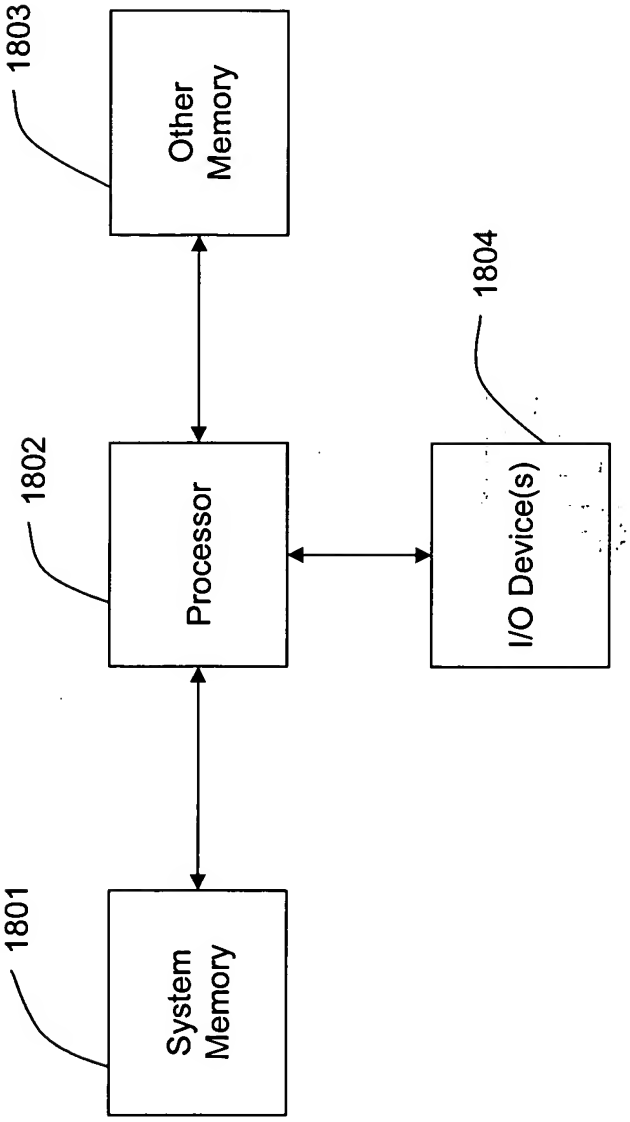

1803
Other Memory
1804
1802
Processor
I/O Device(s)
1801
System Memory

Figure 18